RECEIVED
CENTRAL FAX CENTER
SEP 1 2 2006

In the Claims:

Please amend the claims as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) A phase locked loop comprising a phase detector for determining a phase difference between a reference signal and relative ~~mutually~~ phase shifted signals to generate frequency control signals the phase detector comprising: means for obtaining a one of said frequency control signals by binary multiplication of the reference signal and one of the relative phase signals; ~~and~~ means for obtaining a second one of said control signals by binary multiplication of the relative phase shifted signals, wherein the frequency control signals are coupled to a first charge pump; and a frequency detector coupled to receive the reference signal and the relative phase shifted signals for supplying up and down frequency detector signals to a second charge pump communicatively coupled to a loop filter, the frequency detector comprising a first flip-flop and a second flip-flop each communicatively coupled to the reference signal and to a different one of the relative phase shifted signals and a third flip-flop communicatively coupled to the output of the first and second flip-flops.

2. (Currently Amended) A phase locked loop as claimed in claim 1, further comprising a splitter for generating the relative phase shifted signals the splitter having an input signal generated by a voltage controlled oscillator coupled to the first charge pump and to a ~~the~~ low-pass filter.

3. (Currently Amended) A phase locked loop as claimed in claim 2, wherein the splitter comprises a binary divider receiving the input ~~a~~ signal generated by the voltage controlled oscillator and generating a binary signal used as a clock signal for a divide by two circuit comprising a first bi-stable circuit ring-coupled to a second bi-stable circuit for generating the relative phase shifted signals.

4. (Original) A phase locked loop as claimed in claim 2, wherein the splitter comprises a series coupling of a delay line and an inverter.

5. (Original) A phase locked loop as claimed in claim 2, wherein the voltage controlled oscillator is a quadrature oscillator generating signals that are in quadrature to each other, and the relative phase shifted signals being in quadrature.

6. (Currently Amended) A phase locked loop as claimed in claim 1, ~~further~~ wherein ~~comprising a~~ the ~~frequency detector~~ up and a down frequency detector signals are generated using a binary multiplication of a signal from the output of the second flip-flop and a signal from the output the first flip-flop. ~~coupled to receive the reference signal and the relative phase shifted signals for supplying an up frequency detector signal[(]) and a down charge pump coupled to the loop filter~~.

7. (Currently Amended) A phase locked loop ~~as claimed in claim 6,~~ comprising a phase detector for determining a phase difference between a reference signal and relative phase shifted signals to generate frequency control signals the phase detector comprising: means for obtaining a one of said frequency control signals by binary multiplication of the reference signal and one of the relative phase signals; means for obtaining a second one of said control signals by binary multiplication of the relative phase shifted signals; and a frequency detector coupled to receive the reference signal and the relative phase shifted signals for supplying an up frequency detector signal and a down charge pump coupled to the loop filter, wherein the frequency detector comprises a third flip-flop and a fourth flip-flop driven by the reference signal and having at their inputs the relative phase signals, outputs of the third and fourth flip-flops being coupled to input terminals of a fifth flip-flop the phase detector generating the up frequency detector signal obtained by binary multiplication between a signal generated by the fifth flip-flop at ~~it's~~ its output and the signal obtained at the bar-output of the fourth flip-flop, and further generating the down frequency detector signal obtained by binary multiplication of the signal obtained at a bar-output of the fourth flip-flop and the signal obtained at a bar-output of the fifth flip-flop signal obtained at the bar-output of the fourth flip-flop.

8. (New) For use in a phase locked loop having a reference signal and relative phase shifted signals, a method for generating frequency control signals used by a first charge pump and frequency detector signals for a second charge pump communicatively coupled to a loop filter, the method comprising:

obtaining one of said frequency control signals by binary multiplication of the reference signal and one of the relative phase signals;

obtaining a second one of said control signals by binary multiplication of the relative phase shifted signals; and

obtaining up and down frequency detector signals using a first, second and third flip-flop each of the first and second flip-flops communicatively coupled to the reference signal and to a different one of the relative phase shifted signals and a third flip-flop communicatively coupled to the output of the first flip-flop and the output of the second flip-flop.

9. (New) For use in a phase locked loop having a reference signal and relative phase shifted signals, a method for generating frequency control signals used by a first charge pump and frequency detector signals for a second charge pump communicatively coupled to a loop filter, the method comprising:

obtaining one of said frequency control signals by binary multiplication of the reference signal and one of the relative phase signals;

obtaining a second one of said control signals by binary multiplication of the relative phase shifted signals; and

obtaining up and down frequency detector signals using a first, second and third flip-flop each of the first and second flip-flops communicatively coupled to the reference signal and to a different one of the relative phase shifted signals and a third flip-flop communicatively coupled to the output of the first flip-flop and the output of the second flip-flop, wherein the reference signal drives the first and second flip-flops, the relative phase signals drive inputs of the first and second flip-flops, outputs of the first and second flip-flops being coupled to input terminals of the third flip-flop, the up frequency detector signal is obtained by binary multiplication between a signal generated by the third flip-flop at its output and a signal obtained at the bar-output of the

second flip-flop, and the down frequency detector signal is obtained by binary multiplication of the signal obtained at a bar-output of the second flip-flop and a signal obtained at a bar-output of the third flip-flop signal obtained at the bar-output of the second flip-flop.